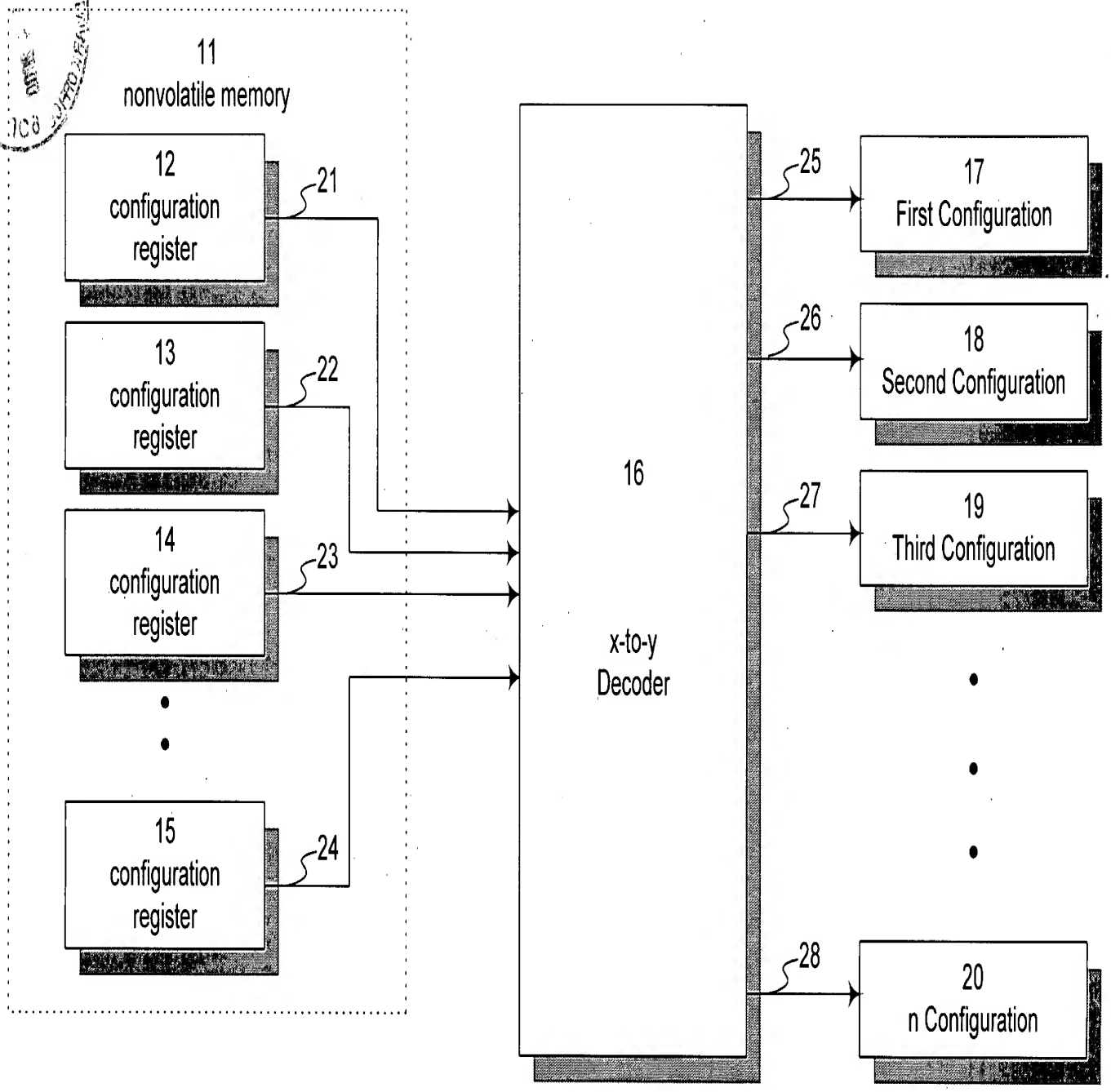

FIG. 1

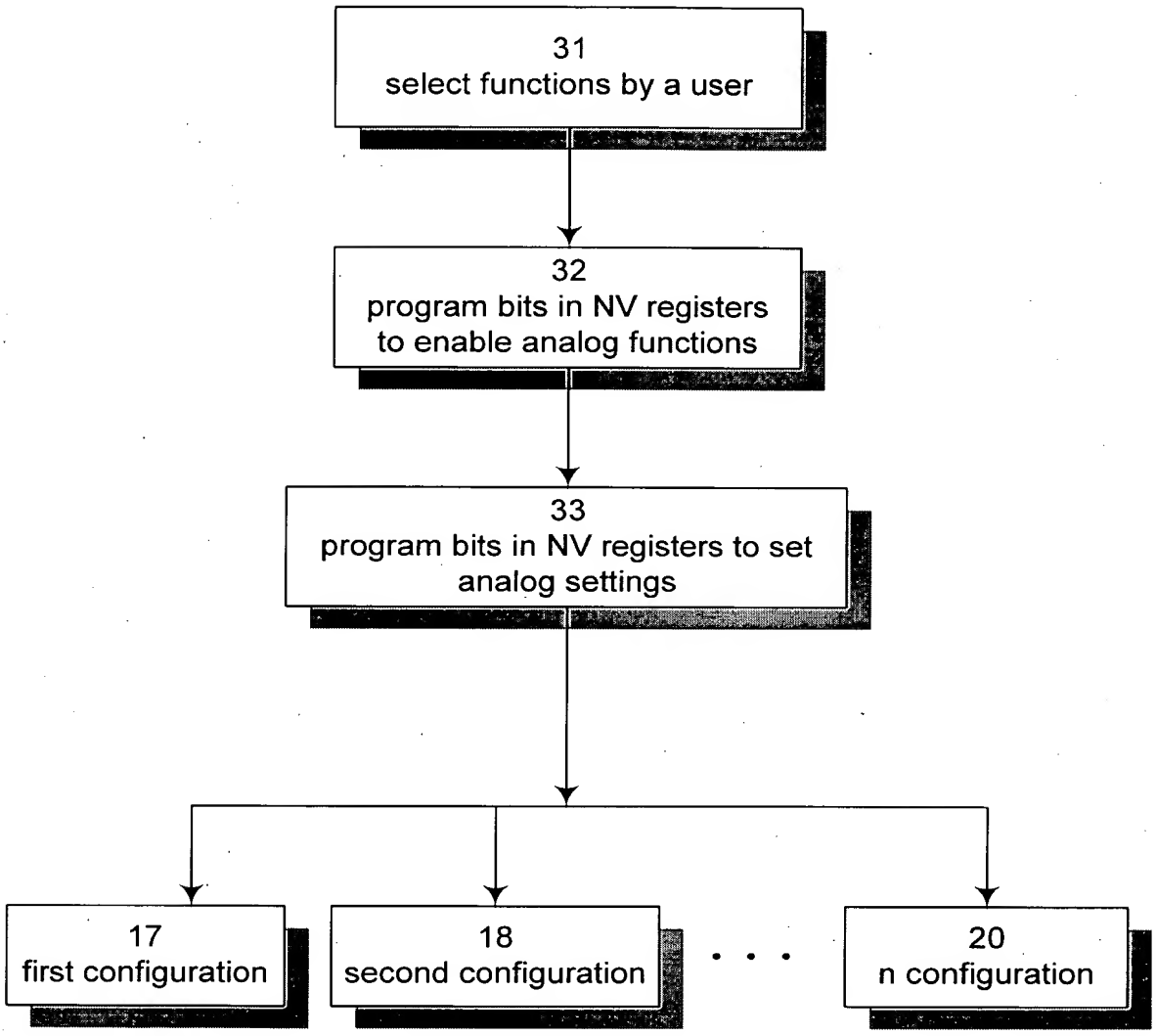
31
select functions by a user
32
program bits in NV registers to enable analog functions
33
program bits in NV registers to set analog settings
17
first configuration
18
second configuration
20
n configuration
30

FIG. 2

Byte 0

Bits 6-5	Reset timout	Bits 4-0	Reset range
11	200ms	10000	4.625
10	100ms	01000	4.375
01	50ms	00100	2.9
00	25ms	00010	2.65
		00001	2.15

FIG. 3A

Byte 1

Bit 6	Complete config write disable	Bit 5	Vsense overvoltage/ undervoltage	Bit 4	Responds to all addresses
1	Write disable	1	Undervoltage	1	Respond to all addresses
0	Write enable	0	Overvoltage	0	Respond to pin addresses

Bit 3	Change device identifier code	Bit 2-0	Watchdog interval
1	Respond to 1011	111	6.4s
0	Respond to 1010	110	3.2s
		101	1.6s
		100	.8s
		011	.4s
		00X	off

FIG. 3B

Byte 2

Bits 7-5	Osc Trim	Bit 4	Full Mem/ Half Mem	Bits 3-0	Bandgap (Vsense) trim
111	Slower	1	4K/16K	1111	Lower
000	Faster	0	2K/8K	0000	Higher

FIG.3C

Byte 3

Bits 7	Config write disable	Bits 6-4	Full Mem/ Half Mem	Bits 3-0	Vtrip trim
1	Write disable	111	Part 8	1111	Lower
0	Write enable	110	Part 7	0000	Higher
		101	Part 6		
		100	Part 5		
		011	Part 4		
		010	Part 3		
		001	Part 2		
		000	Part 1		

FIG. 3D

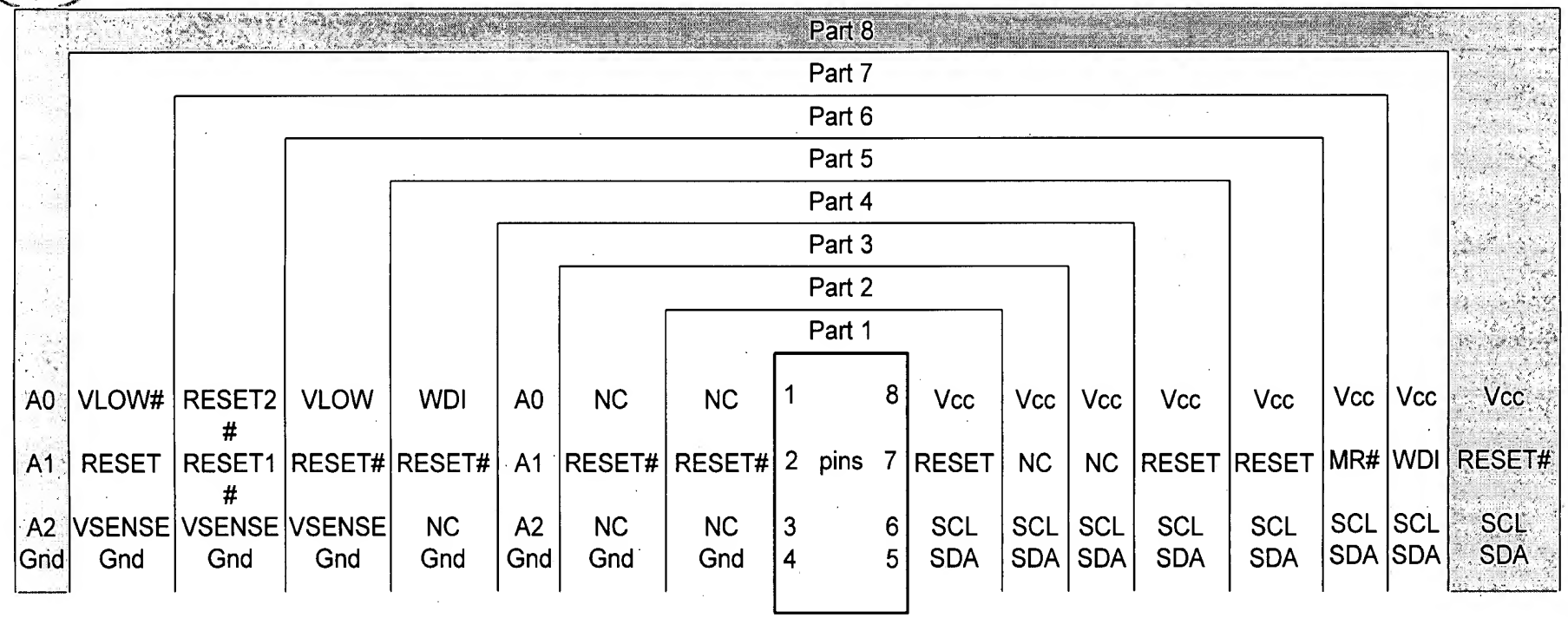
Part 8
Part 7
Part 6
Part 5
Part 4
Part 3
Part 2
Part 1
A0 VLOW# RESET2# VLOW WDI A0 NC NC 1 8 Vcc Vcc Vcc Vcc Vcc Vcc Vcc Vcc
A1 RESET RESET1# RESET# RESET# A1 RESET# RESET# 2 pins 7 RESET NC NC RESET RESET MR# WDI RESET#
A2 VSENSE VSENSE VSENSE NC A2 NC NC 3 6 SCL SCL SCL SCL SCL SCL SCL SCL
Gnd Gnd Gnd Gnd Gnd Gnd Gnd Gnd 4 5 SDA SDA SDA SDA SDA SDA SDA SDA

FIG. 4

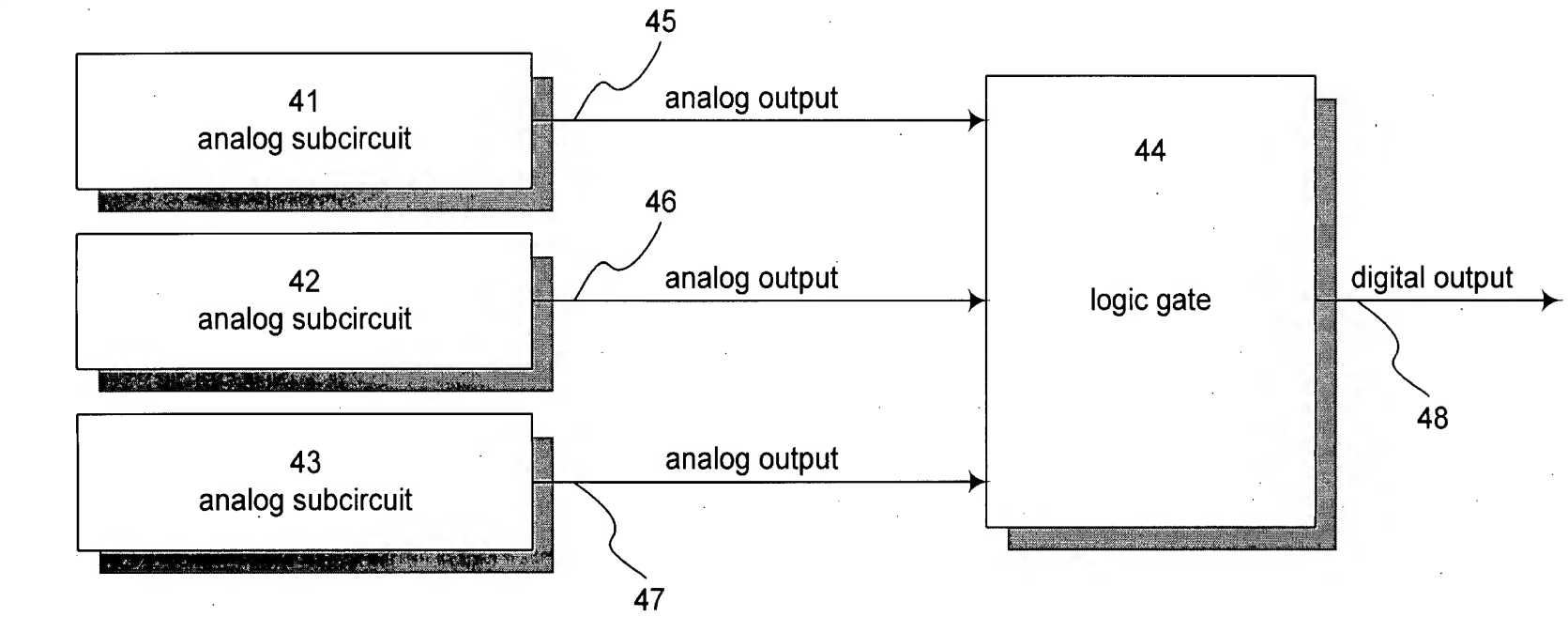
45
41
analog subcircuit
analog output
44
46
42
analog subcircuit
analog output
logic gate
digital output
48
43
analog subcircuit
analog output
47
40

FIG. 5